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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/574,653	05/18/2000	Youngmin Kim	TI-29012	8503

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EXAMINER	
LEE, HSIEN MING	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/574,653	Applicant(s) KIM ET AL.	
	Examiner Hsien-Ming Lee	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) 13-19 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicants' election without traverse to claims 1-12 is acknowledged. Applicants are reminded to cancel non-elected claims 13-19.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 4-12 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

In light of claim body in claim 4, lines 6-7, 15-20 and Fig. 1C, the sidewall width (102) of the transistor having the *opposite* type of conductivity (such as n-type) with respect to that of a substrate (such as p-type) is less than that of the transistor having the same type of conductivity as of substrate. However, the limitations " forming ..... a **second** width adjacent to said **first** transistor gate stack wherein said second width is **less** than said **first** width" , as recited in claim 4, lines 26-29, **contradict** to what are recited in claim 4, lines 6-7, 15-20 and Fig. 1C. The same errors also occur in claims 9-12.

The Examiner has presumed that the limitations " forming at least ..... wherein said second width is less than said first width", as recited in **claim 4, lines 26-29**, should be -- forming at least ..... wherein said second width is **larger** than said first width.---

Furthermore, the limitations " masking said second transistor .....etching said sidewalls of a first width adjacent to said first transistor .... thereby forming sidewalls of a second width adjacent to said first transistor ...", as recited in **claim 9, line 31 of page 13 through line 4 of page 14**, should be --- masking said **first** transistor .....etching said sidewalls of a first width adjacent to said **second** transistor .... thereby forming sidewalls of a second width adjacent to said **second** transistor ---.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-6, 8-10 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Ogoh (US 5,254,866).

With respect to claims 1-3, Ogoh in Fig.5 A-5F and related text on col. 5, lines 53-63 and col. 10, lines 11-21, identically teaches the claimed method of forming a CMOS sidewall spacer, comprising the steps of:

- forming a PMOS transistor gate structure 16/18 on a n-type region 14 of a semiconductor substrate 11;
- forming a NMOS transistor gate structure 17/15 on a p-type region 13 of the semiconductor substrate 11;

- forming sidewall structures 21/27/41 (oxide) adjacent to the NMOS and 22/28/42 adjacent to the PMOS transistor gate structure; and
- anisotropically etching the sidewall structure adjacent to the NMOS such that the sidewall width adjacent to the NMOS is less than the sidewall width adjacent to the PMOS (col. 5, lines 53-63 and col.10, lines 11-21).

With respect to claims 4-6, 8-10 and 12, Ogoh in Fig.5 A-5F and related text on col. 5, lines 53-63 and col. 10, lines 11-21, also identically teaches the claimed method of forming a CMOS sidewall spacer, comprising the steps of:

- providing a semiconductor substrate of a first conductivity type such as p-type (col. 2, lines 36-46) with a region of a second conductivity type such as n-type region 14;
- forming a gate dielectric 15/16 on the semiconductor substrate 11;
- forming a conductive layer 17/18 on the gate dielectric 15/16;
- etching the conductive layer 17/18 and the gate dielectric 15/16 to form a first transistor gate stack 16/18 (PMOS) with an upper surface on the semiconductor substrate of a first conductivity (p-type) and a second transistor gate stack 17/15 (NMOS) with an upper surface on the semiconductor substrate of a second conductivity type (n-type);
- forming a sidewall film (oxide) over the semiconductor substrate;
- anisotropically etching the sidewall film such that all of the sidewall film is removed from the upper surface of the first transistor gate stack and the upper surface of the second transistor gate stack, wherein a plurality of sidewall structure of a first width 22/28 are formed adjacent to the first transistor gate stack 16/18 (PMOS), and a

plurality of sidewall structure of a first width 21/27 are formed adjacent to the second transistor gate stack 15/17 (NMOS) (Fig.5C);

- masking the first transistor gate stack 16/18 with a photoresist pattern 23 used for source drain implantation (Fig. 5C);
- etching the sidewalls of the first width adjacent to the second transistor gate stack 15/17 (NMOS) thereby forming sidewalls of a second width adjacent to the second transistor gate stack 15/17 (NMOS) wherein the second width is less than the first width, i.e. the **sidewall width of the second transistor (NMOS) is less than sidewall width of the first transistor (PMOS)** (col. 5, lines 53-63 and col.10, lines 11-21).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogoh ('866) in view of Wang et al. (US 6,020,231).

Ogoh fails to teach utilizing a plasma etch process as the anisotropical etching for forming the sidewalls at both sides of the CMOS. However, the plasma etch is a well-known practice for etching a sidewall film to form the sidewalls of the CMOS, as evidenced by Wang et al., in which they states that " a conventional fabrication technique for forming such side wall

spacer is by way of CVD forming of an oxide layer, and a subsequent step of anisotropic etching, typically either reactive ion etching or plasma etching." (col. 1, lines 40-43).

Therefore, it would have been obvious to artisan to use the plasma etch process of Wang et al. to anisotropically etch the sidewall film of Ogoh to form the sidewalls of the CMOS, since the plasma etch process is a reliable method for selective etching with good dimension control.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-0142 for regular communications and 703-305-0142 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Hsien Ming Lee
March 20, 2002

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800